BYPASS SWITCH TOPOLOGY FOR LOW-NOISE AMPLIFIERS

Abstract of the Disclosure

A bypass switch topology for a low-noise amplifier is provided. In one aspect of the invention, an amplifier includes at least one signal amplifying transistor, coupled between an input terminal and an output terminal associated with the amplifier, for amplifying a received input signal. The amplifier also includes a bypass switch, coupled to the at least one signal amplifying transistor, for providing a gain (e.g., high-gain) mode operation and a bypass mode operation, the bypass switch including two transistors. In the gain mode operation, the two transistors of the bypass switch are off and the at least one signal amplifying transistor amplifies the received input signal and passes the amplified signal to the output terminal. In the bypass mode operation, the two transistors of the bypass switch are on, the at least one signal amplifying transistor is turned off, and the received input signal is passed directly from the input terminal to the output terminal.